

ERRATA

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Candidate

FOR

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for TPM 2.0**

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1. Introduction

This document describes errata and clarifications for the TCG PC Clients Specific Platform TPM Profile (PTP) for TPM 2.0 v1.03 revision 22 as published. The information in this document is likely – but not certain – to be incorporated into a future version of the specification. Suggested fixes proposed in this document may be modified before being published in a later TCG Specification. Therefore, the contents of this document are not normative and only become normative when included in an updated version of the published specification. Note that since the errata in this document are non-normative, the patent licensing rights granted by Section 16.4 of the Bylaws do not apply.

2. Clarifications

2.1 Clarification 1

In Section 5.5.3.8, the informative Figure 4 – TPM State Diagram for CRB Interface contains typographic errors. State transitions 26 and 27a are described as completing the state transition within TIMEOUT_E. TIMEOUT_E is not defined. The correct timeout should be TIMEOUT_C.

2.2 Clarification 2

In Section 5.5.2.5.2 Bus Access of the Status Register, the Bit Field: resetEstablishmentBit is subject to the same reset timing as the rest of the Status register as outlined in Section 6.6 normative 2.

3. Errata

3.1 Errata 1

In Section 3.2, Table 2, the comment for TPM_ALG_AES incorrectly includes 256-bit keys as necessary minimum support. This revision of the specification should be interpreted to require support for only 128-bit AES keys.

3.2 Errata 2

Section 5.5.3.2.1 Table 24 TPM_LOC_STATE is incorrectly identified as an 8-bit register. However, Table 10 and Table 23 define this register as a 4-Byte or 32-bit register. The additional bits should be interpreted to be reserved and, following the defined behavior for reserved fields, would return all 0's on reads. The register definition in Table 24 may be extended in a future revision of the specification to include the additional 3 Bytes defined for this register in Table 10 and Table 23.

3.3 Errata 3

Section 8.1 Table 60 – QFN-32 Pin Assignments does not include Pin 8 in the VDD row, however, pin 8 is identified in Figure 23 as being connected to VDD. The Figure is correct and the Table entry should be interpreted as the Figure is defined.